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04/03/2006 TOKON1 00000003 500220 10808007
01 FC:1251 120.00 CR

Attorney's Docket No. 9060-228

PATENT MAINTENANCE
DIVISION
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2006 APR 20 PM 4:16

In re: Esa Paatero

Confirmation No.: 5679

Serial No.: 10/808,007

Examiner: Rajnikant B. Patel JS PATENT & TRADEMARK

Filed: March 24, 2004

Group Art Unit: 2838 OFFICE

For: POWER CONVERSION APPARATUS WITH DC BUS PRECHARGE CIRCUITS AND
METHODS OF OPERATION THEREOF

April 17, 2006

Mail Stop 16

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

**REQUEST FOR REFUND OF FEE
UNDER 37 C.F.R. §1.26**

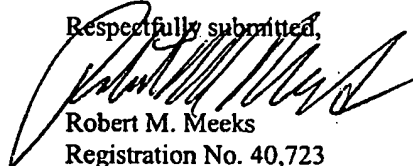
Sir:

Applicants respectfully submit this Request for Refund of Fees pursuant to 37 C.F.R. §1.26 in the amount of \$120.00. Our Deposit Account No. 50-0220 was charged a \$120.00 extension of time fee on April 3, 2006 (copy enclosed as Appendix A). A Response to Restriction was filed on March 24, 2006 and was acknowledged as received in the U.S. Patent and Trademark Office on March 28, 2006 on the stamped return postcard (copy enclosed as Appendix B).

According to the February 10, 2006 Office Action Summary (copy enclosed as Appendix C), the deadline for filing a response to the Office Action "... is set to expire 3 month(s) or thirty (30) days, whichever is longer, from the mailing date of this communication" (i.e., May 10, 2006).

Thus, Applicants do not believe that the \$120.00 extension of time fee is required. Accordingly, please credit our Deposit Account No. 50-0220 in the amount of \$120.00 to refund this overpayment of fees.

Respectfully submitted,



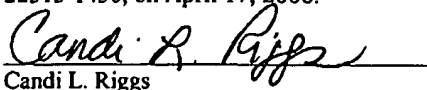
Robert M. Meeks

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop 16, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 17, 2006.



Candi L. Riggs

APPENDIX A



**United States
Patent and
Trademark Office**

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Deposit Account Statement

Requested Statement Month: April 2006
 Deposit Account Number: 500220
 Name: MYERS BIGEL SIBLEY & SAJOVEC, P.A.
 Attention: ACCOUNTING DEPT
 Address: P O BOX 37428
 City: RALEIGH
 State: NC
 Zip: 27627
 Country: UNITED STATES OF AMERICA

DATE	SEQ	POSTING REF TXT	ATTORNEY DOCKET NBR	FEE CODE	AMT	BAL
04/03	4	10808007	9060-228	1251	\$120.00	\$44,764.00
04/03	10	10561688		9204	-\$100.00	\$44,864.00
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04/03	19	60007749	9301-39PR	8021	\$40.00	\$44,784.00
04/03	22	60007749	9301-39PR	8021	\$40.00	\$44,744.00
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04/03	34	08654453	9301-1	8021	\$40.00	\$44,624.00
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04/03	51	11313039	9301-1	8021	\$40.00	\$43,944.00
04/03	52	11313572	9301-1	8021	\$40.00	\$43,904.00
04/03	53	11374191	9301-1	8021	\$40.00	\$43,864.00
04/03	54	60760432	9301-1	8021	\$40.00	\$43,824.00
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04/03	64	10225615	9301-1	1501	\$1,400.00	\$42,384.00

APPENDIX B

M.S. Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

RMM/clv

Date: 3/24/06

Doc. No. 9060-228

Serial No. 10/808,007

Inventor: Esa Paterno

Sir: Kindly acknowledge receipt of the accompanying items listed below
by placing your receiving stamp hereon and return mailing:

<input type="checkbox"/> Application Transmittal and	<input type="checkbox"/> Check \$
<input type="checkbox"/> Specification pages	<input type="checkbox"/> IDS & PTO-1449 & refs.
<input type="checkbox"/> No. of Claims	<input type="checkbox"/> Amendment & Amend. Transmittal
<input type="checkbox"/> Declaration & POA	<input type="checkbox"/> Preliminary Amendment
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<input type="checkbox"/> Formal Drawings/ sheets	<input type="checkbox"/> Appeal
<input type="checkbox"/> Associate Power of Attorney	<input type="checkbox"/> Submittal of Priority Doc.
<input type="checkbox"/> Exp. Mail	<input type="checkbox"/> 1st Class Mail

✓ Other: Response to Restriction

Respectfully submitted,
MYERS BIGEL SIBLEY & SAJOVEC, P.A.
Attorneys for Applicant

Attorney Docket No. 9060-228

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Esa Paatero
Serial No.: 10/808,007
Filed: March 24, 2004

Group Art Unit: 2838
Examiner: Rajnikant B. Patel
Confirmation No.: 5679

For: POWER CONVERSION APPARATUS WITH DC BUS PRECHARGE CIRCUITS
AND METHODS OF OPERATING THEREOF

Date: March 24, 2006

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

Applicants provide the present Response to Restriction Requirement to address the issues raised in the Office Action mailed February 10, 2006.

If any extension of time for the accompanying response or submission is required, Applicants requests that this be considered a petition therefor. The Commissioner is hereby authorized to charge any additional fee, which may be required, or credit any refund, to our Deposit Account No. 50-0220.

A Listing of Claims is provided for the Examiner's reference beginning on page 2 of this paper.

Remarks/Arguments begin on page 11 of this paper.

Listing of Claims:

1. (Original) A power conversion apparatus comprising:
 - a DC link comprising first and second DC busses and a reference bus;
 - a DC generator circuit coupled to the DC link and operative to generate first and second DC voltages with respect to the reference bus on respective ones of the first and second DC busses; and
 - a precharge circuit coupled to the DC link and operative to charge a first capacitance between the first DC bus and the reference bus and to transfer charge from the charged first capacitance to a second capacitance between the second DC bus and the reference bus.
2. (Original) An apparatus according to Claim 1, wherein the DC generator circuit is operative to commence generation of the first and second DC voltages on the first and second DC busses after the precharge circuit precharges the first and second DC busses.
3. (Original) An apparatus according to Claim 1, wherein the precharge circuit comprises:
 - a precharge converter circuit operative to charge the first capacitance from an AC source and/or a DC source; and
 - a balancer circuit operative to transfer charge between the first and second capacitances.
4. (Original) An apparatus according to Claim 3, wherein the balancer circuit is operative to selectively couple the first and second DC busses to the reference bus via an inductor.

5. (Original) An apparatus according to Claim 4, wherein the balancer circuit comprises:

an inductor; and

first and second switches operative to selectively couple respective ones of the first and second DC busses to the inductor.

6. (Original) An apparatus according to Claim 5, further comprising a third switch operative to couple and decouple the inductor to and from the reference bus.

7. (Original) An apparatus according to Claim 3, wherein the DC generator circuit and the balancer circuit include a common half-bridge circuit.

8. (Original) An apparatus according to Claim 7, wherein the common half-bridge circuit is configurable to operate as a rectifier circuit in a first mode of operation and as a balancer circuit in a second mode of operation.

9. (Original) An apparatus according to Claim 1, wherein the precharge circuit is operative to charge the first capacitance to increase a voltage between the first DC bus and the reference bus to a first voltage and to initiate charge transfer to the second capacitance after the voltage between the first DC bus and the reference bus reaches the first voltage.

10. (Original) An apparatus according to Claim 9, wherein the precharge circuit is further operative to terminate charge transfer to the second capacitance after a voltage between the second DC bus and the reference bus reaches a second voltage.

11. (Original) An apparatus according to Claim 10, wherein the DC generator circuit is operative to generate the first and second DC voltages on the first and second DC busses from an AC source, and wherein the second voltage is greater than a peak voltage of the AC source.

18. (Original) An apparatus according to Claim 1, further comprising first and second storage capacitors coupled between respective ones of the first and second DC busses and the reference bus, and wherein the first and second capacitances comprise respective ones of the first and second storage capacitors.

19. (Original) A power conversion apparatus comprising:
a DC bus;
a buck converter circuit coupled to the DC bus and operative to charge a capacitance coupled to the DC bus; and
a boost converter circuit coupled to the DC bus and operative to commence generating a DC voltage on the DC bus from an AC source and/or a DC source after the precharge circuit precharges the DC bus.

20. (Original) A power conversion apparatus, comprising:
a DC link comprising first and second DC busses and a reference bus;
a boost converter circuit coupled to the DC link and operative to generate first and second DC voltages with respect to the reference bus on respective ones of the first and second DC busses from an AC source and/or a DC source; and
a precharge circuit coupled to the DC link and operative to charge a first capacitance between the first DC bus and the reference bus and to transfer charge from the charged first capacitance to a second capacitance between the second DC bus and the reference bus.

21. (Original) An apparatus according to Claim 20, wherein the boost converter circuit is operative to commence generation of the first and second DC voltages on the first and second DC busses after the precharge circuit precharges the first and second DC busses.

22. (Original) An apparatus according to Claim 20, wherein the precharge circuit comprises:
a buck converter circuit operative to charge the first capacitance; and
a balancer circuit operative to transfer charge between the first and second capacitances.

23. (Original) An apparatus according to Claim 22, wherein the boost converter circuit and the balancer circuit include a common half-bridge circuit.

24. (Original) An apparatus according to Claim 23, wherein the common half-bridge circuit is configurable to operate as a boost rectifier circuit in a first mode of operation and as a balancer circuit in a second mode of operation.

25. (Original) An uninterruptible power supply (UPS) comprising:
a DC link comprising first and second DC busses and a reference bus;
a DC generator circuit coupled to the DC link and operative to generate first and second DC voltages with respect to the reference bus on respective ones of the first and second DC busses from either or both of a first power source and a second power source; and
a precharge circuit coupled to the DC link and operative to charge a first capacitance between the first DC bus and the reference bus and to transfer charge from the charged first capacitance to a second capacitance between the second DC bus and the reference bus.

26. (Original) A UPS according to Claim 25, wherein the DC generator circuit is operative to commence generation of the first and second DC voltages on the first and second DC busses after the precharge circuit precharges the first and second DC busses.

27. (Original) A UPS according to Claim 25, wherein the precharge circuit comprises:

a precharge converter circuit operative to charge the first capacitance from an AC source and/or a DC source; and

a balancer circuit operative to transfer charge between the first and second capacitances.

28. (Original) A UPS according to Claim 27, wherein the DC generator circuit comprises a boost converter circuit and wherein the precharge converter circuit comprises a buck converter circuit.

29. (Original) A UPS according to Claim 27, wherein the DC generator circuit and the balancer circuit include a common half-bridge circuit.

30. (Original) A UPS according to Claim 29, wherein the common half-bridge circuit is configurable to operate as a rectifier circuit in a first mode of operation and as a balancer circuit in a second mode of operation.

31. (Original) A UPS according to Claim 25, wherein precharge circuit is operative to charge the first capacitance to increase a voltage between the first DC bus and the reference bus to a first voltage and to initiate charge transfer to the second capacitance after the voltage between the first DC bus and the reference bus reaches the first voltage.

32. (Original) A UPS according to Claim 31, wherein the precharge circuit is further operative to terminate charge transfer to the second capacitance after a voltage between the second DC bus and the reference bus reaches a second voltage.

33. (Original) A UPS according to Claim 32, wherein the DC generator circuit is operative to generate the first and second DC voltages on the first and second DC busses from an AC source, and wherein the second voltage is greater than a peak voltage of the AC source.

34. (Original) A UPS according to Claim 32, wherein the precharge circuit is further operative to initiate charge transfer from the charged second capacitance to the first capacitance to further boost the voltage between the first DC bus and the reference bus.

35. (Original) A UPS according to Claim 25, wherein the precharge circuit is operative to charge the first capacitance from the first power source and/or the second power source.

36. (Original) A UPS according to Claim 25, wherein the first power source comprises an AC power source and wherein the second power source comprises a DC power source.

37. (Original) A UPS according to Claim 36, wherein the DC power source comprises a battery.

38. (Original) A UPS according to Claim 25, further comprising first and second storage capacitors coupled between respective ones of the first and second DC busses and the reference bus, and wherein the first and second capacitances comprise respective ones of the first and second storage capacitors.

39. (Original) A UPS according to Claim 25, further comprising a DC/AC converter circuit coupled to the DC link and operative to generate an AC voltage from the first and second DC voltages.

40. (Original) A method of operating a power converter including a DC link comprising first and second DC busses and a reference bus and a DC generator circuit coupled to the DC link and operative to generate first and second DC voltages with respect to the reference bus on respective ones of the first and second DC busses, the method comprising:

charging a first capacitance between the first DC bus and the reference bus;
transferring charge from the charged first capacitance to a second capacitance between the second DC bus and the reference bus to charge the second capacitance; and then

generating the first and second DC voltages on the first and second DC busses using the DC generator circuit.

41. (Original) A method according to Claim 40:

wherein charging a first capacitance comprises charging the first capacitance using a buck converter circuit coupled to an AC source and/or a DC source; and

wherein transferring charge comprises transferring charge using a balancer circuit.

42. (Original) A method according to Claim 41, wherein the DC generator circuit and the balancer circuit include a common half-bridge circuit.

43. (Original) A method according to Claim 42:

wherein transferring charge transferring charge from the charged first capacitance to the second capacitance using a balancer circuit comprises transferring charge from the charged first capacitance using the common half-bridge circuit as a balancer circuit; and

wherein generating the first and second DC voltages on the first and second DC busses using the DC generator circuit comprises generating the first and second DC voltages on the first and second DC busses using the common half-bridge circuit as a rectifier circuit.

44. (Original) A method according to Claim 40:

wherein charging the first capacitance comprises charging the first capacitance to increase a voltage between the first DC bus and the reference bus to a first voltage; and

wherein transferring charge from the charged first capacitance to a second capacitance between the second DC bus and the reference bus to charge the second capacitance comprises initiating charge transfer from the charged first capacitance to the second capacitance after the voltage between the first DC bus and the reference bus reaches the first voltage.

45. (Original) A method according to Claim 44, further comprising terminating charge transfer from the first capacitance to the second capacitance after a voltage between the second DC bus and the reference bus reaches a second voltage.

46. (Original) A method according to Claim 45, wherein generating the first and second DC voltages on the first and second DC busses using the DC generator circuit comprises generating the first and second DC voltages on the first and second DC busses from an AC source, and wherein the second voltage is greater than a peak voltage of the AC source.

47. (Original) A method according to Claim 46, wherein generating the first and second DC voltages on the first and second DC busses using the DC generator circuit is preceded by transferring charge from the charged second capacitance to the first capacitance to further boost the voltage between the first DC bus and the reference bus.

48. (Previously Presented) A UPS comprising the power conversion apparatus of Claim 1, wherein the DC generator circuit is operative to generate the first and second DC voltages from either or both of a first power source and a second power source.

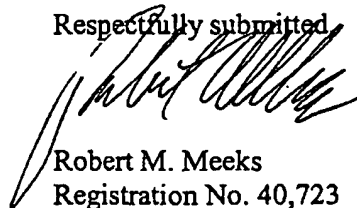
REMARKS

This paper is responsive to the restriction requirement of the Office Action mailed February 10, 2006 (hereinafter "Office Action"). The Office Action identifies two inventions, a Group I (Claims 1-20 and 40-47) drawn to a power conversion apparatus and a Group II (Claims 25-39) drawn to an uninterruptible power supply. Applicant continues to provisionally elect Group II (Claims 25-39), and continues traversal of the restriction requirement, as the Office Action appears to not have made the restriction requirement final.

The Office Action continues to assert "Group I and Group II are related as combination and subcombination." Office Action, p. 2. This is incorrect, as Claim 25 is not a subcombination of Claim 1. As noted in Applicant's prior response filed December 23, 2005, "a combination is an organization of which a subcombination or element is a part." See MPEP 810.05(a). In particular, *Claim 25 contains additional elements to those recited in Claim 1, such that it is not a "part" of Claim 1.* Therefore, Claim 25 is not a subcombination of Claim 1. In fact, as noted in Applicant's prior response, Claim 1 of Group I is a *subcombination* with respect to Claim 25, and the requirements for two-way distinctness between these claims required to support restriction of such a combination/subcombination relationship is not present.

Applicant notes that there is an apparent contradiction between the "Respond to Argument" section and the "Restriction Requirement" section on page 2 of the Office Action. The "Respond to Argument" section appears to acknowledge that Claim 1 stands in relation as a subcombination of the combination recited in Claim 25. However, this appears to be at odds with the combination/subcombination relationship alleged in the "Restriction Requirement" section, which, as noted above, appears to assert that Claim 25 is a subcombination of Claim 1. Applicant also points out that the Office Action omits any requirement regarding Claims 21-24 and 48. Accordingly, if the restriction requirement is maintained, Applicant respectfully requests clarification of the restriction requirement before making such requirement final.

Respectfully submitted,




Robert M. Meeks
Registration No. 40,723

In re: Esa Paatero
Serial No.: 10/808,007
Filed: March 24, 2004
Page 12 of 12

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 24, 2006.



Traci A. Brown

APPENDIX C



UNITED STATES PATENT AND TRADEMARK OFFICE

Rmm

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,007	03/24/2004	Esa Paatero	9060-228	5679

7590 02/10/2006

Robert M. Meeks
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Post Office Box 37428
Raleigh, NC 27627

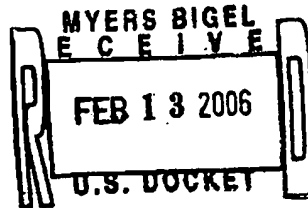
EXAMINER

PATEL, RAJNIKANT B

ART UNIT PAPER NUMBER

2838

DATE MAILED: 02/10/2006



Please find below and/or attached an Office communication concerning this application or proceeding.

02-13-06 A09:21 IN

Office Action Summary	Application No.	Applicant(s)	
	10/808,007	PAATERO, ESA	
	Examiner	Art Unit	
	Rajnikant B. Patel	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2005.
- 2a) ☐ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) 1-47 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 1-47 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |